

USSN 10/608,606

PATENT

-6-

Remarks

Claims 1-19 are pending in the application. Claims 9-11 and 13-18 have been withdrawn from consideration by the Examiner.

I. CLAIM REJECTIONS UNDER 35 USC § 102(e)

Claims 1-7, 12 and 19 are rejected under 35 USC § 102(e) as being anticipated by United States patent application publication no. 2003/0 040 138 of Kobayashi et al. (*Kobayashi*).

A. Claim 1-4

The official action states in part "And, it is noted that the pad 7 therein can be naturally regarded as a mounting pad since at least one terminal of the wire 12 therein is mounted on the pad 7 (see Fig. 15D)." The applicants respectfully disagree with this reading of Kobayashi's disclosure. Kobayashi discloses a die pad 9. The applicants respectfully submit that Kobayashi's die pad 9 can properly be called a "mounting pad" without adopting the tortuous reading proposed in the official action. However, Kobayashi's die pad 9 is not connected by a conductive through hole to an electrode on the rear face of the substrate.

Nevertheless, to avoid confusion the applicants have amended Claim 1 to recite "a conductive die mounting pad."

The applicants respectfully submit that the fabrication of Kobayashi's die pad does not involve the process claimed in Claim 1 as now amended. Moreover, the applicants respectfully submit that Kobayashi neither teaches nor suggests that transistor chip T could be mounted on either of first electrode 7 and second electrode 8, connected by conductive through holes TH to rear face electrodes 10 and 11, respectively. As noted above, Kobayashi teaches mounting transistor chip T on die pad 9, independent of electrodes 7 and 8.

Accordingly, the applicants respectfully submit that Claim 1 as now amended is patentable over Kobayashi.

B. Claims 2-19

The applicants respectfully submit that Claims 2-19 that depend on Claim 1 are

USSN 10/608,606

PATENT

-7-

patentable as a result of the patentability of Claim 1 as now amended.

C. Claims 5-7

The official action states "the layers 20 and 21 in Kobayashi are each readable as a seed layer as the plated portion in the final pads 7 and 10 are respectively plated thereon. And, the method of Kobayashi further comprises: forming the seed layer (20 and/or 21) on the substrate of an unfired ceramic; firing (i.e., sintering) the ceramic after drilling the hole(s) therein; and forming additional layers (the plated portion, see Paragraph 0016) on the seed layers after the firing."

The applicants respectfully disagree with the reading of Kobayashi's disclosure. Kobayashi's Figures 15A-15D show a first embodiment based on a glass-epoxy substrate and Kobayashi describes a method of fabricating the glass-epoxy-based embodiment with reference to the right-hand column of Figure 16. Additionally, Kobayashi describes a method of fabricating a second embodiment based on a ceramic substrate with reference to the right-hand column of Figure 16. Figure 16 clearly shows that different fabrication processes are used to fabricate the glass-epoxy-based embodiment and the ceramic-based embodiment. For example, the through-hole is formed the glass-epoxy-based embodiment after the copper foil layers have been applied to the substrate, whereas the through-hole is formed in the ceramic-based embodiment before the conductive layers have been printed on the substrate.

In the rejection quoted above, the Examiner takes features from the fabrication method of the glass-epoxy-based embodiment and applies them to the fabrication method of the ceramic-based embodiment. The applicants respectfully submit that, in a rejection under 35 USC § 102, it is improper to combine features of different embodiments even though the embodiments are disclosed in the same reference. Accordingly, the applicants respectfully submit that the rejection of Claims 5-7 under 35 USC § 102(e) is improper.

D. Claim 6

The applicants respectfully note that the official action does not indicate where in Kobayashi's disclosure can be found a teaching of "filling the through hole in the unfired

USSN 10/608,606

PATENT

-8-

ceramic," as recited in Claim 6. Kobayashi teaches that, after the ceramic substrate has been sintered, the processing of the ceramic substrate is the same as that of the glass-epoxy-based embodiment (paragraph 0019). Accordingly, the applicants respectfully submit that Kobayashi implicitly teaches that the through hole is filled after the ceramic has been sintered, and therefore cannot accurately be said to teach or suggest "filling the through hole in the unfired ceramic," as recited in Claim 6. The applicants therefore respectfully submit that Claim 6 is patentable for this additional reason.

II. CLAIM REJECTION UNDER 35 USC § 103(a)

Claim 8 is rejected under 35 USC § 103(a) as being unpatentable over Kobayashi in view of United States patent no. 5,298,687 of Rapoport et al. (*Rapoport*). The applicants respectfully traverse the rejection on the grounds that the prima facie case of obviousness set forth in the official action does not comply with the requirements set forth in MPEP § 2143.

The official action states that Kobayashi does not expressly disclose that the seed layer can be formed by screen printing and looks to Rapoport for a teaching of the missing element. The official action states:

[I]t is noted that screening printing is one of the art known common methods for forming a seed layer for achieving good plating quality with low cost, as evidenced in Rapoport. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the seed-layer screen-printing step of Rapoport into the method of Kobayashi, so that a method for making a semiconductor device having high quality plated pads therein with low cost would be obtained.

First, the applicants note with regret that the official action does not indicate where in the cited references may be found the motivation set forth in the official action. Specifically, the applicants note that the official action does not indicate where in Kobayashi's disclosure can be found a teaching or suggestion that indicates that the method disclosed therein for depositing conductive material on a ceramic substrate produces inadequate quality or is high in cost. The applicants have been unable to find such teaching. Moreover, the official action does not indicate where in Rapoport's disclosure may be found a teaching or suggestion that Rapoport's interconnection system is capable of producing high-quality plated pads with low cost, as alleged in the official action. Without such teachings in the cited references, the prima facie case of

USSN 10/608,606

PATENT

-9-

obviousness does not comply with the requirements of MPEP § 2143.

Second, the applicants note that the official action does not indicate where in the cited references can be found a teaching that would provide the person of ordinary skill in the art with a reasonable expectation of success in the event such person were to attempt the modification of Kobayashi's manufacturing process proposed in the official action. The applicants have been unable to find such teaching.

Third, for the reasons set forth above with reference to Claim 1 on which Claim 8 depends, the applicants respectfully submit that the proposed combination of references does not disclose all the limitations recited in Claim 8.

Fourth, for the reasons set forth above with reference to Claims 5-7 on which Claim 8 depends, the applicants respectfully submit that the proposed combination of references does not properly disclose all the limitations recited in Claim 8.

Accordingly, the applicants respectfully submit that prima facie case of obviousness set forth in the official action with respect to Claim 8 does not comply with the requirements of MPEP § 2143 because it does not set forth a motivation and a reasonable expectation of success supported by the cited references, and the proposed combination of references does not disclose all the limitations recited in Claim 8.

The applicants respectfully request reconsideration of the rejected claims. The applicants believe that the application as now amended is in condition for allowance, and respectfully request such favorable action. If any matters remain outstanding in the application, the Examiner is respectfully invited to telephone the applicants' attorney at (650) 485-3015 so that these matters may be resolved.

USSN 10/608,606

PATENT

-10-

Respectfully submitted,

Kong Weng Lee et al.

By: 

Ian Hardcastle

Reg. No. 34,075

Dated: 050309

Agilent Technologies, Inc.
Legal Department, MS DL429
P.O. Box 7599
Loveland, CO 80537-0599

Tel.: (650) 485-3015